In the Specification

At page 10, lines 3 – 18, please replace the paragraph as follows (underlined denotes replacements additions and strikethough notes deletions):

As discussed above, the electric field stimulation is applicable to many different devices, such as conventionally packaged dies, flip-chip packaged dies and dies having silicon-on-insulator (SOI) structure. If necessary, a packaged die being analyzed is prepared for the type of analysis to be performed. In one instance, a portion of a packaged die is removed to expose a region in the die via which the electric field is applied. For conventionally packaged dies, this involves applying the electric field via a portion of a chip passivation layer where some of the passivation layer has been removed. For flip-chip packaged dies, a portion of a backside that is opposite a circuit side (arranged face-down on a package substrate) is removed, and the electric field is applied via the removed portion of the backside. For general information regarding implementations to which the present invention is applicable, and for specific information regarding the removal of substrate for preparing a die for analysis in connection with the present invention, reference may be made to U.S. Patent Application Serial No. 09/997,715, now U. S. Patent No. 6,635,572~~(AMDA.504PA/TT4056)~~, filed November 28, 2001 and entitled "Method of Substrate Silicon Removal for Integrated Circuit Devices," which is fully incorporated by reference.

At page 10, lines 19 – 23 and page 11, lines 1 – 7, please replace the paragraph as follows (underlined denotes replacements additions and strikethough notes deletions):

As discussed above, the present invention is applicable to a variety of analysis techniques and to a variety of types of semiconductor dies. FIG. 2 shows one such semiconductor die 200 conventionally packaged to a substrate 202 and undergoing analysis with a scanning probe microscope (SPM) tip 220 (only a portion of which is shown for clarity), according to another example embodiment of the present invention. The die 200 includes a circuit portion 210 located in a die passivation layer 208 of a circuit side of the die. The die is operated and the SPM tip 220 is moved into position over the circuit portion 210 using a circuit diagram of the die for reference. The SPM tip is finely etched to a point having a diameter of less than about 50

nanometers. As the SPM tip is scanned across the circuit portion 210, a change in an electrical characteristic of the die is detected. The electrical characteristic change is used to detect a condition of circuitry in the die, such as a defective circuit.